REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Redrawn with changes. Add device types 03 and 04. Add vendor CAGE 01295. Editorial changes throughout.	94-06-20	M. A. Frye

The original front page of this document has been replaced.

REV																			
SHEET																			
REV	B																		
SHEET	15																		

REV STATUS OF SHEETS														
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
90-10-18

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, RS-485 QUAD DIFFERENTIAL LINE RECEIVER, MONOLITHIC SILICON

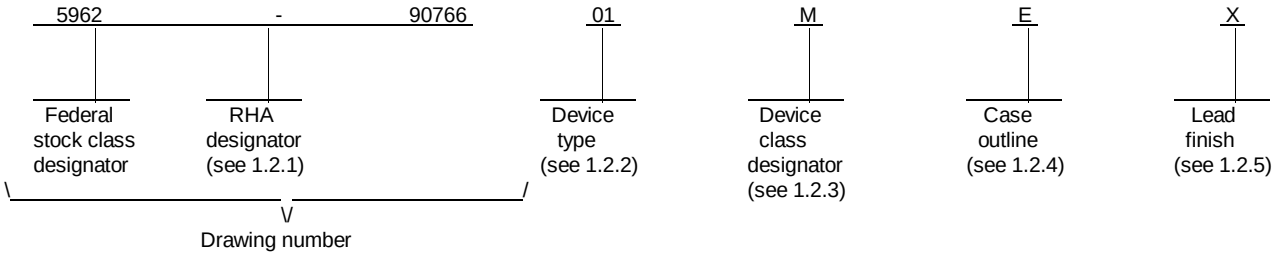
SIZE	CAGE CODE	
A	**67268**	**5962-90766**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	96F175	RS-485 quad differential line receiver
02	96F173	RS-485 quad differential line receiver
03	55LBC175	RS-485 quad differential line receiver, low power
04	55LBC173	RS-485 quad differential line receiver, low power

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	7.0 V dc
Input voltage, A or B inputs (V_{IN})	± 25 V dc
Differential input voltage (V_{ID})	± 25 V dc
Low level output current (I_{OL}):	
Device types 01 and 02	50 mA
Enable input voltage V_{EN}) 2/	7.0 V dc
Storage temperature range	-65° C to 150° C
Lead temperature (soldering, 60 seconds):	
Cases E and F	+300° C
Case 2	+260° C
Junction temperature (T_J)	+150° C
Power dissipation (P_D) 3/:	
Cases E and 2	1375 mW
Case F	1000 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E	100 mW/° C
Case F	145 mW/° C
Case 2	90 mW/° C

1.4 Recommended operating conditions.

Operating supply voltage range (V_{CC}):	
Device types 01 and 02-	4.5 V dc to 5.5 V dc
Device types 03 and 04-	4.75 V dc to 5.25 V dc
Ambient operating temperature range (T_A)	-55° C to +125° C
Common mode input voltage (V_{CM})	-7 V dc to +12 V dc
Output current high (I_{OH}):	
Device types 01 and 02	-400 uA
Device types 03 and 04	8 mA
Output current low (I_{OL}):	
Device types 01 and 02	11 mA

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ V_{EN} applies to device types 02 and 04 only.
3/ Derate above 25° C at 11 mW/° C for case outlines E and 2 and at 8 mW/° C for case outline F.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Supply Current 2/	I_{CC}	V_{ID} = 2 V, V_{CC} = 5.5 V; outputs enabled / outputs disabled	1, 2, 3	01,02		50	mA
		V_{ID} = 5 V, V_{CC} = 5.25 V; outputs enabled / outputs disabled		03,04		20 / 1.4	
Logical "1" output voltage 3/	V_{OH}	I_{OH} = -400 uA, V_{ID} = 0.2 V, V_{CC} = 4.5 V, V_{EN} = 2 V	1, 2, 3	01,02	2.5		V
		I_{OH} = -8 mA, V_{ID} = 0.2 V, V_{CC} = 4.75 V, V_{EN} = 2 V		03,04	3.5		
Logical "0" output voltage 3/	V_{OL}	I_{OL} = 8 mA, V_{ID} = -0.2 V, V_{CC} = 4.5 V, V_{EN} = 2 V	1, 2, 3	01,02		.45	V
		V_{CC} = 4.5 V, I_{OL} = 16 mA, V_{EN}= 2 V, V_{ID} = -0.2 V	1, 3 / 2	03,04		.50 / .70	V
Input threshold voltage 3/ 4/	V_{TH} DIFF	V_O = 2.5 V, V_{CM} = 0 V, I_O = -400 uA	1, 2, 3	01,02		.20	V
		V_O = 3.5 V, V_{CM} = 0 V, I_O = -8 mA		03,04			
		V_O = 2.5 V, V_{CM} = -12 V, I_O = -400 uA		01,02			
		V_O = 3.5 V, V_{CM} = -7 V, I_O = -8 mA		03,04			
		V_O = 2.5 V, V_{CM} = 12 V, I_O = -400 uA		01,02			
		V_O = 3.5 V, V_{CM} = 12 V, I_O = -8 mA		03,04			

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input threshold voltage 3/ 4/	V_{TL} DIFF	V_O = 0.5 V, V_{CM} = 0 V, I_O = 16 mA	1, 2, 3	01,02	-.20		V
			1, 3	03,04			
		V_O = 0.7 V, V_{CM} = 0 V, I_O = 16 mA	2				
		V_O = 0.5 V, V_{CM} = -12 V, I_O = 16 mA	1, 2, 3	01,02			
		V_O = 0.5 V, V_{CM} = -7 V, I_O = 16 mA	1, 3	03,04			
		V_O = 0.7 V, V_{CM} = -7 V, I_O = 16 mA	2				
		V_O = 0.5 V, V_{CM} = 12 V, I_O = 16 mA	1, 2, 3	01,02			
			1, 3	03,04			
		V_O = 0.7 V, V_{CM} = 12 V, I_O = 16 mA	2				
Input line current	I_I	V_{CC} = 4.5 V, V_{IN} = 12 V, untested inputs are 0 V	1, 2, 3	01,02		1	mA
		V_{CC} = 5.5 V, V_{IN} = -7 V, untested inputs are 0 V				-0.8	
		V_{CC} = 5 V and 0 V, V_{IN} = 12 V, untested inputs are 0 V		03,04		1	
		V_{CC} = 5 V and 0 V, V_{IN} = -7 V, untested inputs are 0 V				-0.8	
Logical "1" enable input current	I_{IH}	V_{CC} = 5.5 V, V_{IH} = 2.7 V	1, 2, 3	01,02		10	uA
		V_{CC} = 5.25 V, V_{IH} = 5.0 V		03,04		±20	
Logical "0" enable input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	1, 2, 3	01,02		-100	uA
		V_{CC} = 5.25 V, V_{IN} = 0 V		03,04		-20	
Enable input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_I = -18 mA	1, 2, 3	01,02		-1.5	V
		V_{CC} = 4.75 V, I_I = -18 mA		03,04			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output short circuit current 5/	I_{OS}	V_{CC} = 4.5 V, V_O = 0 V	1, 2, 3	01,02	-85	-15	mA
		V_{CC} = 5.5 V, V_O = 0 V					
		V_{CC} = 4.75 V, V_O = 0 V		03,04		-120	
		V_{CC} = 5.25 V, V_O = 0 V					
High impedance state output current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 0.4 V outputs disabled	1, 2, 3	01,02		±20	µA
		V_{CC} = 5.5 V, V_{OUT} = 2.4 V outputs disabled					
		V_{CC} = 5.25 V, V_{OUT} = 0 V outputs disabled		03,04			
		V_{CC} = 5.25 V, V_{OUT} = 5.25 V outputs disabled					
Logical "1" 6/ enable input voltage	V_{IH}		1, 2, 3	01,02 03,04	2.0		V
Logical "0" 6/ enable input voltage	V_{IL}		1, 2, 3	01,02 03,04		0.8	V
Input resistance	R_{IN}		1, 2, 3	01,02	10		kΩ
Functional test		See 4.4.1.c	7, 8	01,02 03,04			
Propagation delay high to low level output	t_{PHL}	V_{CC} = 5 V, C_L = 15 pF	9	01,02		22	ns
			10, 11			30	
		V_{CC} = 5 V, C_L = 15 pF See figure 3	9	03,04		30	
			10, 11			35	
Propagation delay low to high level output	t_{PLH}	V_{CC} = 5 V, C_L = 15 pF	9	01,02		22	ns
			10, 11			30	
		V_{CC} = 5 V, C_L = 15 pF See figure 3	9	03,04		30	ns
			10, 11			35	
Transition time	t_T	V_{CC} = 5 V, C_L = 15 pF See figure 3	9	03,04		10	ns
			10, 11			16	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Propagation delay output enable time to high level	t_{PZH}	V_{CC} = 5 V, C_L = 15 pF	9	01,02		16	ns
			10, 11			27	
		V_{CC} = 5 V, C_L = 15 pF See figure 3	9	03,04		40	
			10, 11			45	
Propagation delay output enable time to low level	t_{PZL}	V_{CC} = 5 V, C_L = 15 pF	9	01,02		18	ns
			10, 11			27	
		V_{CC} = 5 V, C_L = 15 pF See figure 3	9	03,04		30	
			10, 11			35	
Propagation delay output disable time from high level	t_{PHZ}	V_{CC} = 5 V, C_L = 20 pF	9	01,02		30	ns
			10, 11			37	
		V_{CC} = 5 V, C_L = 5 pF 6/	9			20	
			10, 11			27	
		V_{CC} = 5 V, C_L = 15 pF See figure 3	9	03,04		40	
			10, 11			55	
Propagation delay output disable time from low level	t_{PLZ}	V_{CC} = 5 V, C_L = 5 pF	9	01,02		18	ns
			10, 11			30	
		V_{CC} = 5 V, C_L = 5 pF See figure 3	9	03,04		40	
			10, 11			45	
Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{SK(P)}$	V_{CC} = 5 V, C_L = 15 pF See figure 3	9	03,04		6	
			10, 11			7	
Pulse width	t_{PW}		9	01,02		3	ns
			10			8	
			11			5	

1/ Devices 01 and 03 feature separate active high enables for each receiver pair. Devices 02 and 04 feature an active high and active low enable, common to all four receivers.
2/ ICC is tested with outputs disabled (worse case), ICC enabled is guaranteed by this test. For device types 01 and 02, 4.5 V $\le V_{CC} \le$ 5.5 V and for device types 03 and 04, 4.75 V $\le V_{CC} \le$ 5.25 V.
3/ V_{OH} and V_{OL} are tested over the common mode voltage range of ±12 V for device types 01 and 02 and +12/-7 V for device types 03 and 04 via the V_{TH}/V_{TL} tests.
4/ For this test only, V_{EN} = 2 V for device 01, V_{EN} = 2.5 V and V_{EN} = 0 V for device 02.
5/ Not more than one input should be shorted at a time with duration not to exceed one second.
6/ Guaranteed, if not tested to the limits specified in table I herein.

Device type	01 and 03		02 and 04	
Case outline	E and F	2	E and F	2
Terminal number	Terminal symbol			
1	1B	NC	1B	NC
2	1A	1B	1A	1B
3	1Y	1A	1Y	1A
4	EN1, 2	1Y	EN	1Y
5	2Y	EN1, 2	2Y	EN
6	2A	NC	2A	NC
7	2B	2Y	2B	2Y
8	GND	2A	GND	2A
9	3B	2B	3B	2B
10	3A	GND	3A	GND
11	3Y	NC	$\overline{3Y}$	NC
12	EN3, 4	3B	EN	3B
13	4Y	3A	4Y	3A
14	4A	3Y	4A	$\overline{3Y}$
15	4B	EN3, 4	4B	EN
16	V_{CC}	NC	V_{CC}	NC
17	---	4Y	---	4Y
18	---	4A	---	4A
19	---	4B	---	4B
20	---	V_{CC}	---	V_{CC}

FIGURE 1. Terminal connections.

Device types 01 and 03

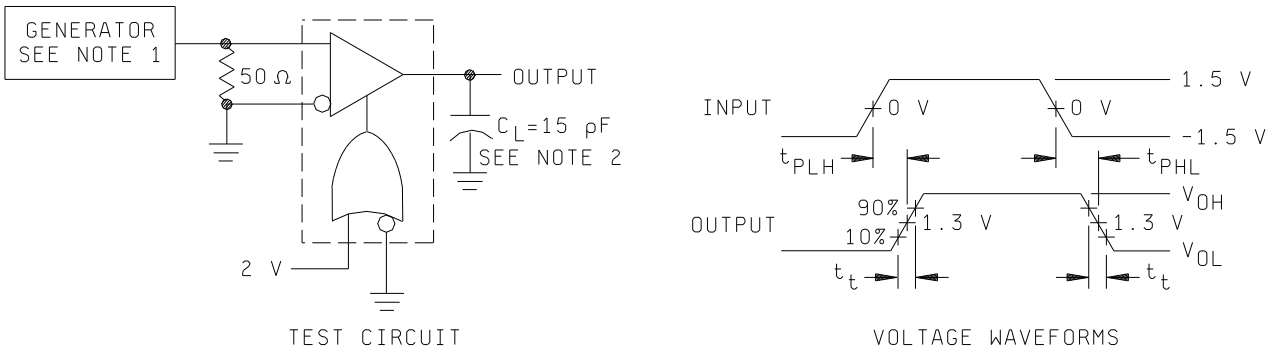
Differential input A - B	Enable EN	Output Y
$V_{ID} \geq +0.2$ V	H	H
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
-0.2 V < V_{ID} < 0.2 V	H	?
Open circuit	H	H

Device types 02 and 04

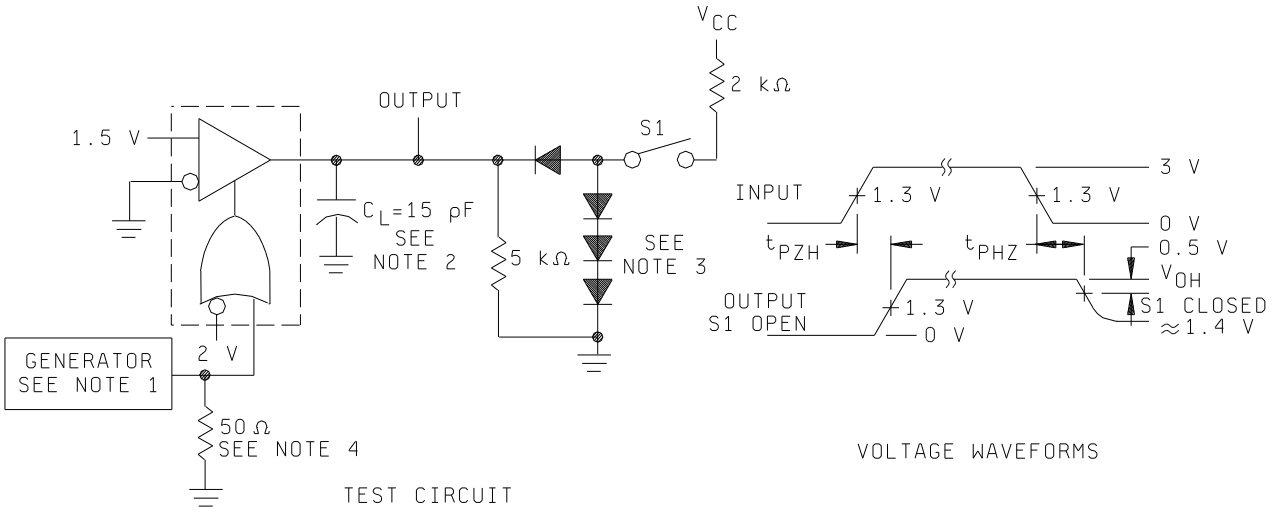
Differential input A - B	Enables EN $\overline{EN}$	Outputs Y
$V_{ID} \geq +0.2$ V	H X X L	H H
$V_{ID} \leq -0.2$ V	H X X L	L L
X	L H	Z
-0.2 V < V_{ID} < 0.2 V	H X X L	? ?
Open circuit	H X X L	H H

X = Don't Care
H = High level
L = Low level
Z = High impedance
? = Indeterminate

FIGURE 2. Truth tables.



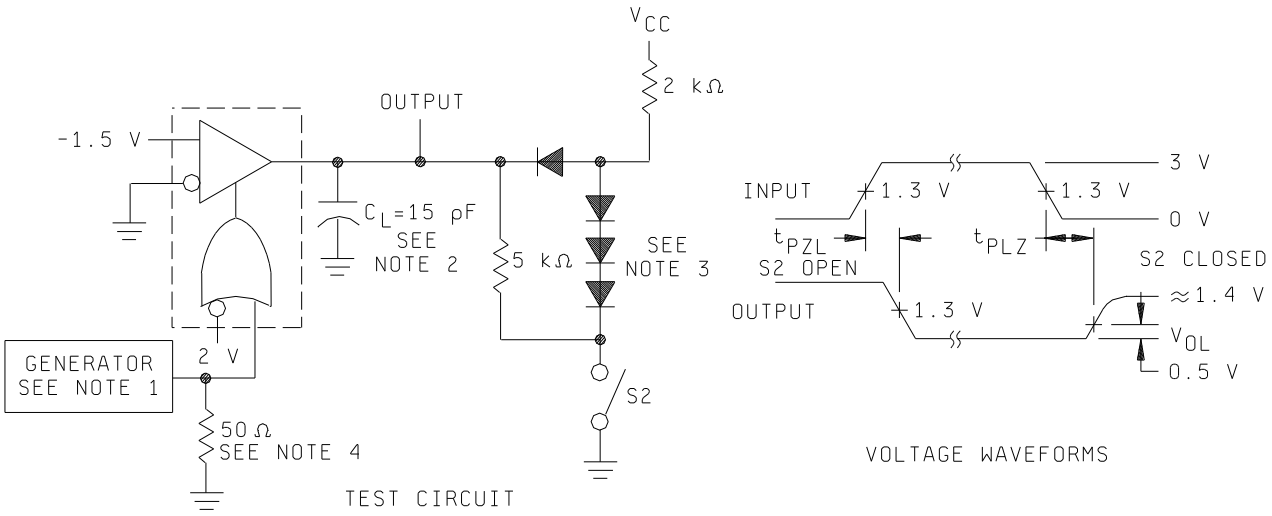
t_{PD} and t_T test circuit and voltage waveforms



t_{PHZ} and t_{PZH} test circuit and voltage waveforms

1/ The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_R ≤ 6 ns, t_F = 6 ns, Z_O = 50 Ω.
2/ C_L includes probe and jig capacitance.
3/ All diodes are 1N916 or equivalent.
4/ To test the active-low enable G, ground G and apply an inverted input waveform to G. $\overline{\text{G}}$

FIGURE 3. Timing diagrams.



t_{PZL} and t_{PLZ} test circuit and voltage waveforms

1/ The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_R ≤ 6 ns, t_F = 6 ns, Z_O = 50 Ω.
2/ C_L includes probe and jig capacitance.
3/ All diodes are 1N916 or equivalent.
4/ To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to G.

FIGURE 3. Timing diagrams - continued.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 53 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125° C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table 1, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 9 1/	1, 2, 3, 9 1/	1, 2, 1/ 3, 9
Group A test requirements (see 4.4)	1, 2, 3, 7 8, 9, 10, 11	1, 2, 3, 7 8, 9, 10, 11	1, 2, 3, 7 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7 ,9	1, 7, 9

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-06-20

Approved sources of supply for SMD 5962-90766 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9076601MEX	27014	DS96F175MJ/883
5962-9076601MFX	27014	DS96F175MW/883
5962-9076601M2X	27014	DS96F175ME/883
5962-9076602MEX	27014	DS96F173MJ/883
5962-9076602MFX	27014	DS96F173MW/883
5962-9076602M2X	27014	DS96F173ME/883
5962-9076603QEX	01295	SNJ55LBC175J
5962-9076603QFX	01295	SNJ55LBC175W
5962-9076603Q2X	01295	SNJ55LBC175FK
5962-9076604QEX	01295	SNJ55LBC173J
5962-9076604QFX	01295	SNJ55LBC173W
5962-9076604Q2X	01295	SNJ55LB173FK

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive PO Box 58090 Santa Clara, CA 95052-8090
01295	Texas Instruments Inc 13500 N Central Expressway PO Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448